The Impact of Grounding Design on Radiated Emissions from Interface Cards

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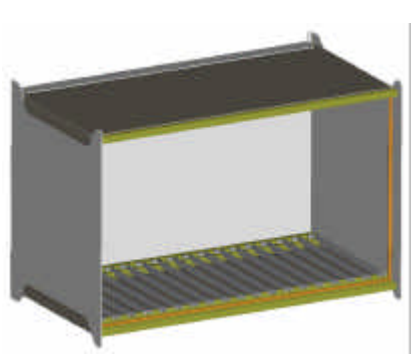
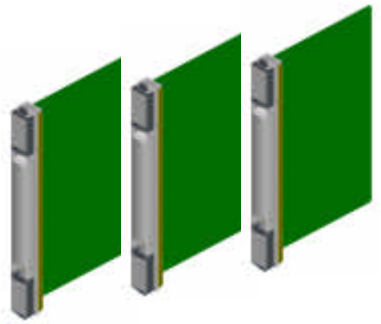
1. Background

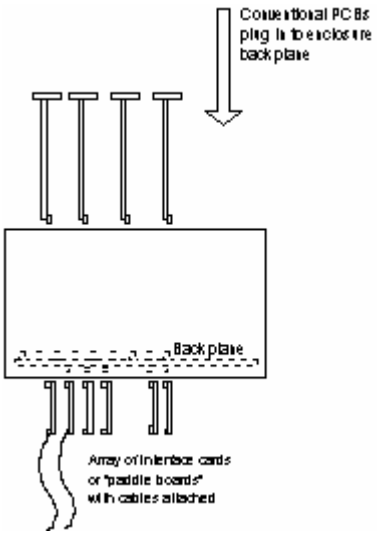
A number of products designed for the Power Utility and telecommunication sectors have to provide a plethora of different electrical interfaces including for example RS232, current loop, E1 (2Mb/s HDB3), Ethernet etc. To reduce design costs, the interface cards are often designed as "add on" PCBs that literally plug in to the rear backplane of a conventional rack as depicted below.

Conventional Rack





Interface or "Paddle Boards" on Rear Backplane



The ground connections (often digital 0V) from the host PCBs to the interface cards are connected via the pin field of various connector families. Data lines and their associated timing signals (clocks) are passed across the interface between the paddle cards and host PCBs. The ground connections between the PCBs are implemented via the connector pin field and can vary significantly in their implementation and concomitant "EMI integrity".

2. EMI Issues

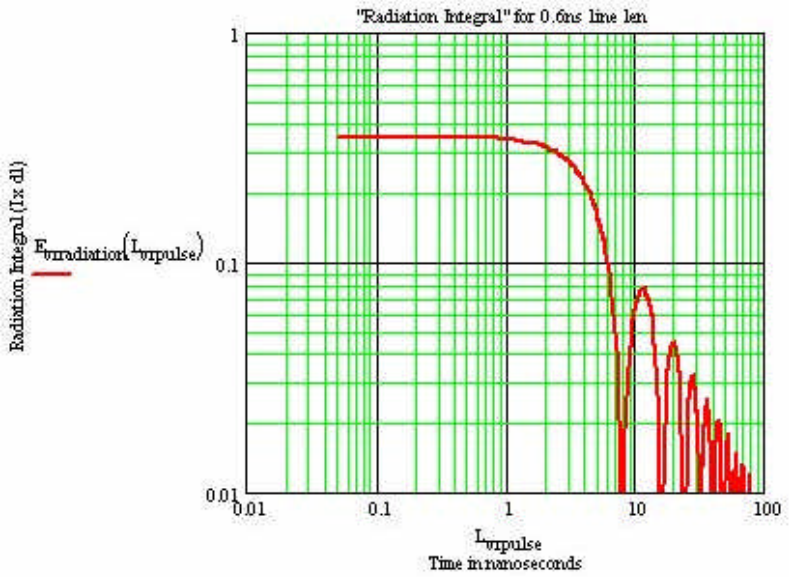
Two EMI phenomenon arise from this grounding implementation. They comprise "ground noise" and direct loop radiated emissions from the currents flowing in the clock and ground return conductors. The ground noise is exacerbated by the copper I/O cables connected to the interface cards and these cables can enhance radiated emissions at the Fourier harmonics of the clock frequency where they become efficient antenna.

3. EMI Analysis

The paper considers the impact of "ground inductance" in the connector pin field. A closed form analysis of ground inductance is made using the concept of "partial self and partial mutual inductance". A new dosed form solution for estimating these parameters has been developed.

An estimate of ground noise current has been computed using a second analytical model that predicts the Fourier current harmonics flowing, as a function of voltage, Z_0 and clock rise time, in a simple series terminated clock line that connects across the host/paddle board interface.

The graph below depicts the quantitative variation in ground noise/radiated emissions as the rise time of the clock waveform is varied over a series terminated line of electrical length 0.6ns. (The x-coordinate parameter depicts clock pulse risetime, the y-coordinate parameter depicts quantitative ground noise levels).



FLO/EMC, a TLM based full field 3D electromagnetic simulator, has been used to model various grounding geometries with the aim of determining the impact on the far field radiation characteristics from each candidate grounding arrangement.

The use of a full field EM simulation tool allows many different candidate grounding arrangements to be studied, and provides additional insight into the frequency response of the system. Various simulations have, and will be performed, looking at both the wideband (so called impulse) response of the system as well as for the spectral response of the associated clock frequencies and various rise times. The impulse response is an especially useful output as it allows for the wideband characteristics of the physical system to be studied. Resonances associated with the physical design of the system will be clearly shown in the response and their relationship to possible clock frequencies can be examined. Through the use of simulation, it is possible to investigate these issues, and others, prior to embarking on the development of physical prototypes.

A hardware demonstrator is being built to facilitate correlation between the measured and simulated results.

The results of the paper are expected to provide an analytical methodology to aid the implementation of a high integrity grounding design between host and interface PCBs. Additionally, FLO/EMC will be able to provide a fast, readily available EMC tool to assess and validate the proposed grounding design strategy for new products. It is anticipated that this combined approach will minimise ground noise radiated emissions from interface/paddle board designs.